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Half Bridge Circuit for Single Phase Active Power Decoupling

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Abstract: Single-phase ac/dc or dc/ac systems are inherently subject to the harmonic disturbance that is caused by the well-known double-line frequency ripple power. This issue can be eased through the installation of bulky electrolytic capacitors in the dc link. Unfortunately, such passive filtering approach may inevitably lead to low power density and limited system lifetime. An alternative approach is to use active power decoupling so that the ripple power can be diverted into other energy storage devices to gain an improved system performance. Nevertheless, all existing active methods have to introduce extra energy storage elements, either inductors or film capacitors in the system to store the ripple power, and this again leads to increased component costs. In view of this, this paper presents a symmetrical half-bridge circuit which utilizes the dc-link capacitors to absorb the ripple power, and the only additional components are a pair of switches and a small filtering inductor. A design example is presented and the proposed circuit concept is also verified with simulation and experimental results. It shows that at least ten times capacitance reduction can be achieved with the proposed active power decoupling method, and both the input current and output voltage of the converter can be well regulated even when very small dc-link capacitors are employed.

Keywords:symmetrical half-bridge circuit, Gird connected systems, Power Factor.

I.INTRODUCTION

The process of improving PF by reducing (Q) is known as Power Factor Correction (PFC).For thetransmission/distribution companies PFC requires the addition of capacitor banks, reactors, phase-shifting transformers, and static VAR compensators to the line, all of which have financial implications. As a result, PFC for household devices has been a necessity in terms of reducing overhead costs and capacity requirements for the transmission/distribution infrastructure.

Examples of industry standards include IEC 61000-3-2 and IEEE STD 519 [5] that determines PF, Total Harmonic Distortion (THD), and harmonic regulation limits. THD measures the purity of the sinusoidal current drawn from the line, and harmonic regulation limits set the maximum allowable signal power for a given harmonic frequency. An example of a consumer PFC rectifier is the bulky external-supply of a laptop attainment system.

In [6], PF of 0.999 and efficiency of 98% is achieved for the consumer power level of 150 W. Since good efficiency has been achieved with current PFC rectifiers, the focus on research is on size reduction, such that PFC rectifiers become more affordable in a wider range of applications. An increasingly popular trend is to use Gallium Nitride High Electron Mobility Transistors (GaN HEMT), as they have intrinsically superior semiconductor properties to that of Silicon (Si) [7]. GaN devices can be used to switch power converters at higher frequencies with better efficiency for improved form factor.

II. SIMULATION

Table 1Key components for the experimental prototype

Sr.No	Component	Description
1	Diode rectifier bridge	GBPC2506,25A/600V,MULTICOMP
2	$Q_1,\ldots Q_3/D_1$	IKW30N60T,30A/600V,INFINEON
3	L_{in}/L_f	200 turns,2×AWG#16,Core DT400-40,DMEGC
4	C_1/C_2	MKP1847630354Y5,30µF/350V,VISHAY
5	C_{dc}	EETED2W471LJ,470µF/450V,PANASONIC

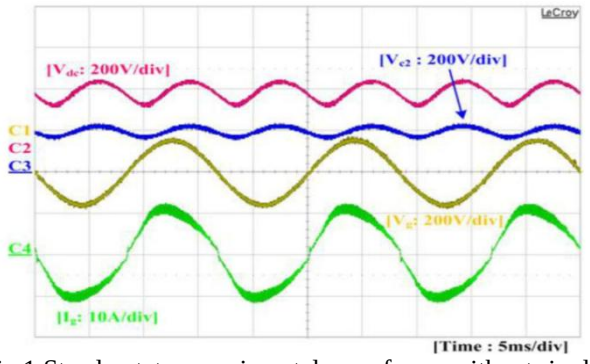

Fig.1.Steady-state experimental waveforms without ripple power compensation. From top to bottom, dc-link voltage, lower capacitor voltage, grid voltage, and grid current.

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It is noted to have approximately π/4 phase shift with the grid voltage, which matches well with the theoretical analysis. A 1-kW prototype was built in the laboratory and the circuit parameters are basically the same as those used in simulation. Two 90-μF film capacitors, each of them consisting of three 30-μF film capacitors in parallel, are connected in series in the dc link and the equivalent dc-link capacitance is only 45 μF, which is much smaller than that of a conventional PFC converter. The key active and passive components used for the tested prototype are summarized in Table II. Fig. 2 shows the steady-state experiments results when the closed-loop controller is disabled and there is no active power decoupling in the circuit. It is obvious that the dc-link contains high ripple voltage because of the very low capacitance, and this ripple voltage in turn affects the regulation of the input current. Even though a second-order notch filter is implemented in the PFC voltage control loop, it is still not enough to attenuate the voltage harmonic disturbance and it fails to provide a clean reference for the inner current control loop. The grid current is therefore seriously distorted by the third-order harmonic with amplitude of 0.92A. The total harmonic distortion (THD) of grid current, calculated up to 100th harmonics, is found to be 9.1%.

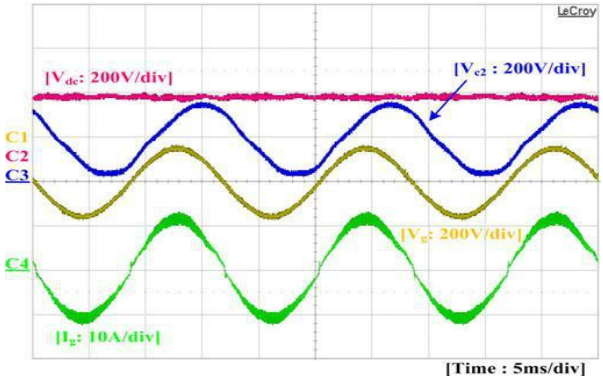

Fig.2 Steady-state experimental waveforms with ripple power Compensationfrom top to bottom, and grid current

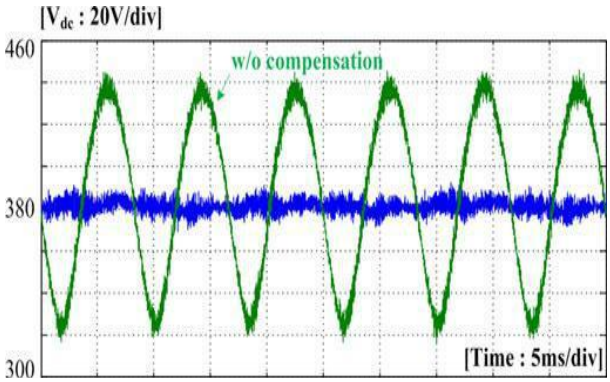

Fig.3 Zoom-in view of the dc-link voltage under two tests

Fig. 2 shows the steady-state experimental results when the, proposed decoupling method is enabled and it is clear that the dc-link voltage ripple can be dramatically reduced. As a consequence, the grid current is also greatly improved and the third harmonic current is reduced to 0.15A only. In this case, the THD of the grid current is improved to 3.8%. Also as anticipated, the capacitor voltage is sinusoidal with Vdc/2 offset, and there is approximately one-eighth cycle phase difference with the grid voltage, which is in good agreement with the theoretical analysis and simulation results presented previously.

Fig. 3 shows the zoom-in view of the dc-link voltage under these two tests. Without compensation, the peak-to-peak dc-link voltage can be up to 120 V, which corresponds to 31.6% of the nominal dc bus voltage, while this ripple voltage can be suppressed to around 10 V, less than 3% of the nominal value if the proposed compensation is implemented. Fig. 4 shows the spectrum of the dc-link voltage and it is clear that there is a dramatic reduction of the second-harmonic voltage after activation of the harmonic distortion.

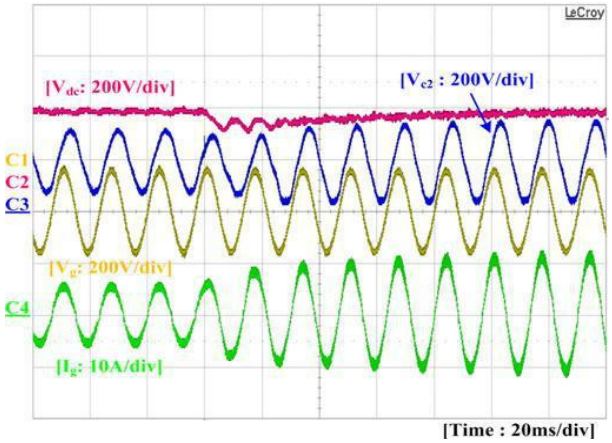

Fig. 4 Dynamic experimental waveforms showing 50% to 100% step-up load change. From top to bottom, dc-link voltage, lower capacitor voltage, grid voltage, and grid current.

The fourth and sixth-harmonic voltages are also slightly reduced due to the improved grid current. The smooth dc-link voltage indicates that ten times capacitance reduction in single-phase systems is successfully achieved with the proposed active power decoupling circuit. The prototype was also tested with dynamic loads and the corresponding load step-up and step-down experimental results are presented in Figs. 4 and 5, respectively.

As shown, the dc-link voltage dip/swell during load transients can be kept within • 100 V. This is acceptable considering the very low equivalent dc-link capacitance used in the circuit. The dc-link voltage canconverge to its nominal value within five line cycles and there is no obvious distortion occurred in the grid current and the power factor is clearly always unity regardless of the load disturbances. This again confirms the effectiveness of the proposed circuit and control algorithm.

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Comparative Study

The proposed single-phase converter is also compared with a conventional boost PFC converter whose dc-link voltage is in order to obtain a similar level of voltage ripple.

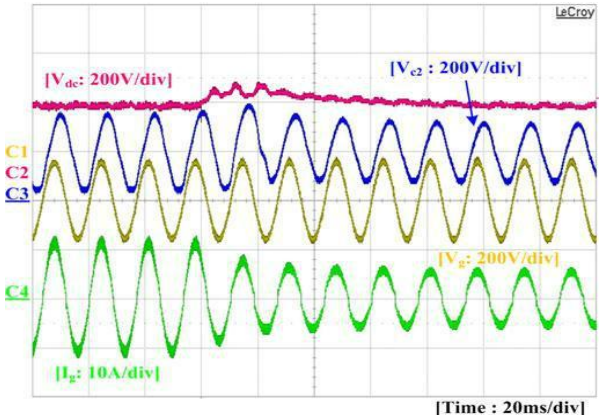

Fig.5 Dynamic experimental waveforms showing 100% to 50% step-down load change. From top to bottom, dc-link voltage, lower capacitor voltage, grid voltage, and grid current.

The required dc-link capacitance, according to (13) will be 920 μF, which is more than 20 times of the proposed system. In experiment, two 470-μF/450-V electrolytic capacitors are used in parallel in the dc link. However, the measured dc-link capacitance is only 840 μF because of the tolerance of the capacitors. It is also clear that the efficiency drop may become more severe at light load as the modulation index of the symmetrical half-bridge is very small during such operating conditions. Efficiency drop is the main drawback of the proposed system and a possible solution could be to use advanced wide band gap case and therefore, the heating effect can be basically neglected. Table III compares the capacitive energy storage requirement for some common active power decoupling circuits. It should be noted that the ωnCV 2 dc term makes no physical meaning and ωn used here is just a scaling factor for assessing the capacitance requirement, because it is quite intuitive that the higher the fundamental frequency, the lower the capacitance can be used in the dc link to obtain the same level of voltage ripple. The circuit in [19] and the proposed consist circuit actually exhibit the same capacitive energy storage requirement because for both of them, the ripple power is stored in the decoupling capacitors as pure ac form (the dc offset voltage in the proposed circuit is not for power decoupling purpose).

The former one has slightly higher requirement because it is installed with more capacitance in the dc link and therefore, it has relatively longer holdup time in case of ac input lost. The proposed circuit may clearly stand out from the existing active power decoupling methods because the film capacitors used in the system are not only for power decoupling, but also for holding up the dc bus voltage, and therefore, the system will be more cost-effective.

III.IMPLEMENTED MATLAB MODEL AND RESULTS

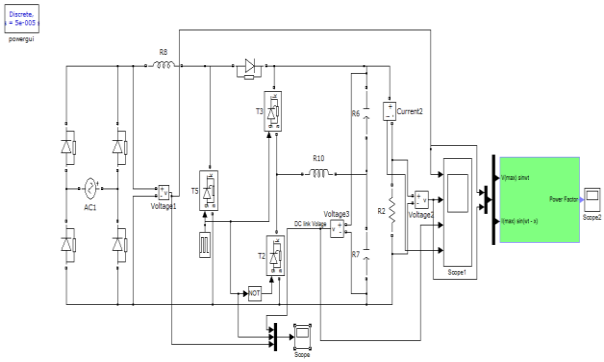

Fig.6 Implementedmodel in MATLAB simulation

Simulation was done in MATLAB/Simulink environment and the key circuit parameters are summarized in Table I. Fig. 1 shows the steady-state simulation results which are comparable to those presented in Fig. 1. Thanks to the smooth dc-link voltage, the input line current can be well regulated by the PFC controller, and it is sinusoidal and in phase with the grid voltage. The two film capacitors can provide the required double-line frequency harmonic power, and the resultant output power can be almost constant. The dc-link voltage has very slight voltage variation, which is around 10 V, and this is caused by the inaccurate calculation of the voltage reference and the errors in the closed-loop control. As mentioned in [19], some closed-loop modifications can be applied to fine tune the voltage reference and to achieve more precise power decoupling. However, this may further complicate the control system, and thus not implemented here.

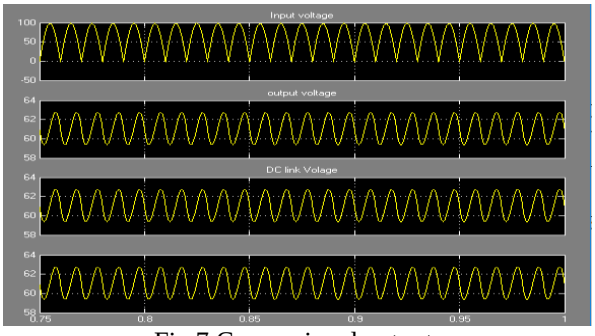

Fig.7 Conversional output

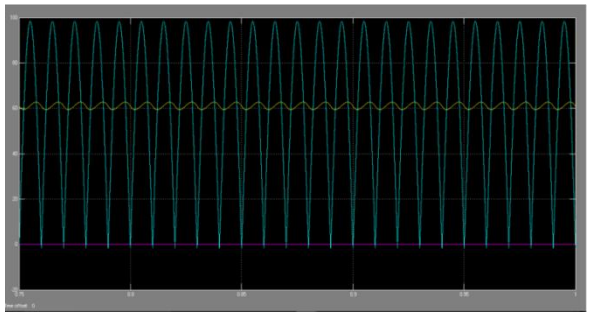

Fig.8 Rectification outputs

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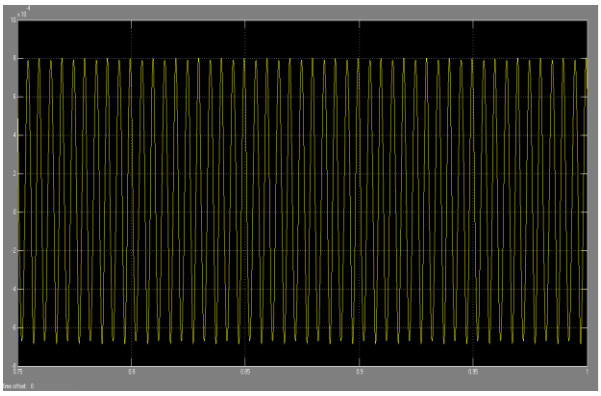

Fig.9 power Factor measurement output

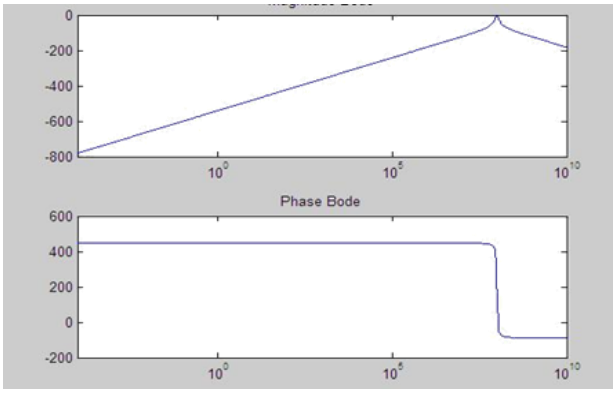

Fig.10 Proposed LC filter output

IV. CONLCUSION

This paper has presented a symmetrical half-bridge circuit to decouple the fluctuating power in single-phase ac/dc and dc/ac systems. The dc-link capacitors in the proposed system may not only provide a high-voltage dc bus to support power conversion, but also absorb the system ripple power originated from the ac side. The resulting system is more cost-effective as compared to other existing active power decoupling methods because it does not need additional passive components to store the system ripple energy. Experimental results under both steady-state and dynamic operations were obtained from a 1-kW PFC prototype and it shows that at least ten times capacitance reduction can be achieved by the proposed active power decoupling circuit. The ripple voltage in the dc link as well as the THD of the gird current can be significantly reduced, which proves the effectiveness of the proposed solution. The proposed symmetrical half-bridge can also be regarded as a generic converter cell and might be a promising solution for elimination of the fluctuating power and the reduction of dc-link capacitance in other advanced topologies, e.g., NPCs and MMCs. Improving the quality of input current to the mains is important in order to meet some forcing standards, such as IEC 61000-3-2 and IEEE 519. Poor quality of input current significantly affects the power factor of the input power and the problem is alleviated by employing PFC circuit as a front- end in a single phase or three phase AC–DC converter. Active PFC technique which operates in CCM is used to achievebetter power factor from the converter. Boost type is preferred to reduce EMI as compared to other types of active PFC.

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